CLAIMS

What is claimed is:

1. An integrated circuit (IC) comprising:

a plurality of circuit rows, at least one row of said plurality of circuit rows including three or more voltage islands;

at least one low voltage island in said at least one row, circuit elements in each said at least one low voltage island being powered by a low voltage (V_{ddl}) supply; and

at least one high voltage island in said at least one row, circuit elements in each said at least one high voltage island being powered by a high voltage (V_{ddh}) supply, V_{ddh} being a higher voltage than V_{ddl}.

2. An IC as in claim 1 wherein said at least one low voltage island is a low voltage macro.

3. An IC as in claim 1 wherein said at least one low voltage island is a low voltage latch.

4. An IC as in claim 1 wherein said at least one low voltage island is a low voltage cell.

5. An IC as in claim 1 wherein said at least one low voltage island spans two or more of said plurality of circuit rows.

6. An IC as in claim 5 wherein said at least one low voltage island is surrounded by a plurality of high voltage islands.

7. An IC as in claim 6 wherein said plurality of high voltage island include a high voltage standard cell, a high voltage latch and a high voltage macro.

8. An IC as in claim 1 wherein said at least one high voltage island includes at least one level converter receiving an output from said at least one low voltage island.

9. An IC as in claim 8 wherein said at least one low voltage island comprises a plurality of low voltage islands and said at least one level converter comprises a plurality of level converters in said high voltage island receiving outputs from said plurality of low voltage islands.

10. A method of reducing power in an integrated circuit (IC) design, said method comprising the steps of:

a) placing and wiring circuit elements for timing closure at a first supply voltage;

b) assigning a plurality of circuit elements for replacement as low voltage circuit elements in a logic aware supply voltage assignment, wherein said low voltage circuit elements operate at a supply voltage below said first supply voltage;

c) optimizing level converter placement; and

d) adjusting assignment of low voltage circuit elements responsive to cell placement in a physically aware voltage re-assignment.

11. A method as in claim 10 further comprising repeating steps (b) – (d) until no circuit elements are assigned for replacement in assigning step (b) and no assignment adjustment is needed in assignment adjusting step (d).

12. A method as in claim 11, further comprising the steps of:

e) placing a power grid to form placed cells in a high and low voltage islands; and

f) passing said placed design to a physical synthesis engine.

13. A method as in claim 10 wherein the logic aware placement in step (b) comprises the steps of:

i) identifying ones of said circuit elements with timing slack; and

ii) selectively replacing identified said ones with low voltage equivalent circuit elements.

14. A method as in claim 13 wherein circuit elements include one or more macros, a plurality of latches and a plurality of cells and the logic aware assignment step (b) further comprises placing level converters at selected outputs of replaced said low voltage macros, said low voltage latches and said low voltage cells.

15. A method as in claim 13 wherein the steps (ii) of selectively replacing said identified ones comprises the steps of:

A) selecting a candidate from said identified ones

B) replacing said candidate with a low voltage equivalent circuit element;

C) checking a timing specification for said candidate; and

D) determining whether said low voltage equivalent meets said timing specification.

16. A method as in claim 15 wherein when said low voltage equivalent fails to meet said timing specification in step (D), said method further comprises reverting the replaced said low voltage equivalent to said circuit element selected as said candidate.

17. A method as in claim 16 further comprising:

E) determining whether any candidates remain unchecked; and

F) selecting an unchecked said candidate and returning to step (B) until all candidates are determined checked in step (E).

18. A method as in claim 17 wherein a plurality of said circuit elements are latches and the step (D) of determining whether latch candidates meet said timing specification comprises determining if all input low voltage latch input pins still have positive slack and whether the output pin slack exceeds a minimum threshold.

19. A method as in claim 18 wherein said minimum threshold exceeds the delay for a level converter.

20. A method as in claim 10 wherein the physically aware voltage reassignment step (d) comprises determining a physical adjacency metric (PAM) for each said low voltage circuit element and reverting all cells with a PAM less than a selected threshold.

21. A method as in claim 10 wherein an input netlist, technology definition and timing constraints are provided for placing and wiring step (a).

22. A computer program product for integrated circuit (IC) design, said computer program product comprising a computer usable medium having computer readable program code thereon, said computer readable program code comprising:

computer program code means for placing and wiring circuit elements for timing closure at a first supply voltage;

computer program code means for a logic aware supply voltage assignment identifying and assigning a plurality of circuit elements for replacement as low voltage circuit elements, wherein said low voltage circuit elements operate at a supply voltage below said first supply voltage;

computer program code means for optimizing level converter placement; and

computer program code means for physically aware voltage re-assignment adjusting assignment of low voltage circuit elements responsive to cell placement.

23. A computer program product as in claim 22, further comprising:

computer program code means for placing a power grid to form placed cells in a high and low voltage islands; and

computer program code means for passing said placed design to a physical synthesis engine.

24. A computer program product as in claim 22, wherein the computer program code means for logic aware placement comprises:

computer program code means for identifying ones of said circuit elements with timing slack; and

computer program code means for selectively replacing identified said ones with low voltage equivalent circuit elements.

25. A computer program product as in claim 24, wherein circuit elements include one or more macros, a plurality of latches and a plurality of cells and said computer program code means for logic aware assignment step further comprises computer program code means for placing level converters at selected outputs of replaced said low voltage macros, said low voltage latches and said low voltage cells.

26. A computer program product as in claim 24 wherein said computer program code means for selectively replacing said identified ones comprises:

computer program code means for selecting a candidate from said identified ones

computer program code means for replacing said candidate with a low voltage equivalent circuit element;

computer program code means for checking a timing specification for said candidate; and

computer program code means for determining whether said low voltage equivalent meets said timing specification.

27. A computer program product as in claim 26 wherein said computer program code means for determining when said low voltage equivalent fails to meet said timing specification further comprises computer program code means for reverting replaced said low voltage equivalents to said circuit elements selected as said candidates.

28. A computer program product as in claim 27 wherein a plurality of said circuit elements are latches and said computer program code means for determining whether candidates meet said timing specification comprises determining for said latches if all input low voltage latch input pins still have positive slack and whether latch output pin slack exceeds a minimum threshold.

29. A computer program product as in claim 28 wherein said minimum threshold exceeds the delay for a level converter.

30. A computer program product as in claim 22 wherein said computer program code means for physically aware voltage re-assignment comprises:

computer program code means for determining a physical adjacency metric (PAM) for each said low voltage circuit element; and,

computer program code means for reverting all cells with a PAM less than a selected threshold.

31. A computer program product as in claim 22 further comprising computer program code means for receiving an input netlist, technology definition and timing constraints for a design.